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FACULTY OF ENGINEERING & TECHNOLOGY

BCS-501 Operating System

Lecturer-27

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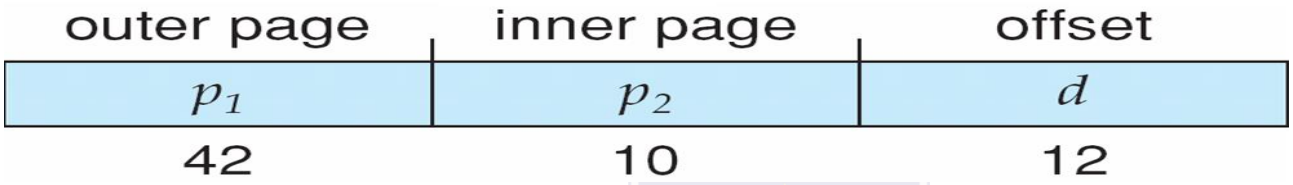
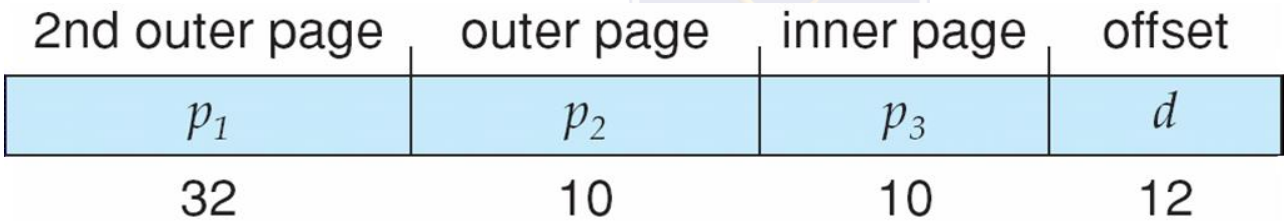
Paging Scheme

- Three-level Paging Scheme
- Hashed Page Tables
- Inverted Page Table
- Inverted Page Table Architecture

Paging Scheme

Three-level Paging Scheme:---





Hashed Page Tables

•Common in address spaces > 32 bits

•The virtual page number is hashed into a page table

- ➢This page table contains a chain of elements hashing to the same location

•Each element contains (1) the virtual page number (2) the value of the mapped page frame (3) a pointer to the next element

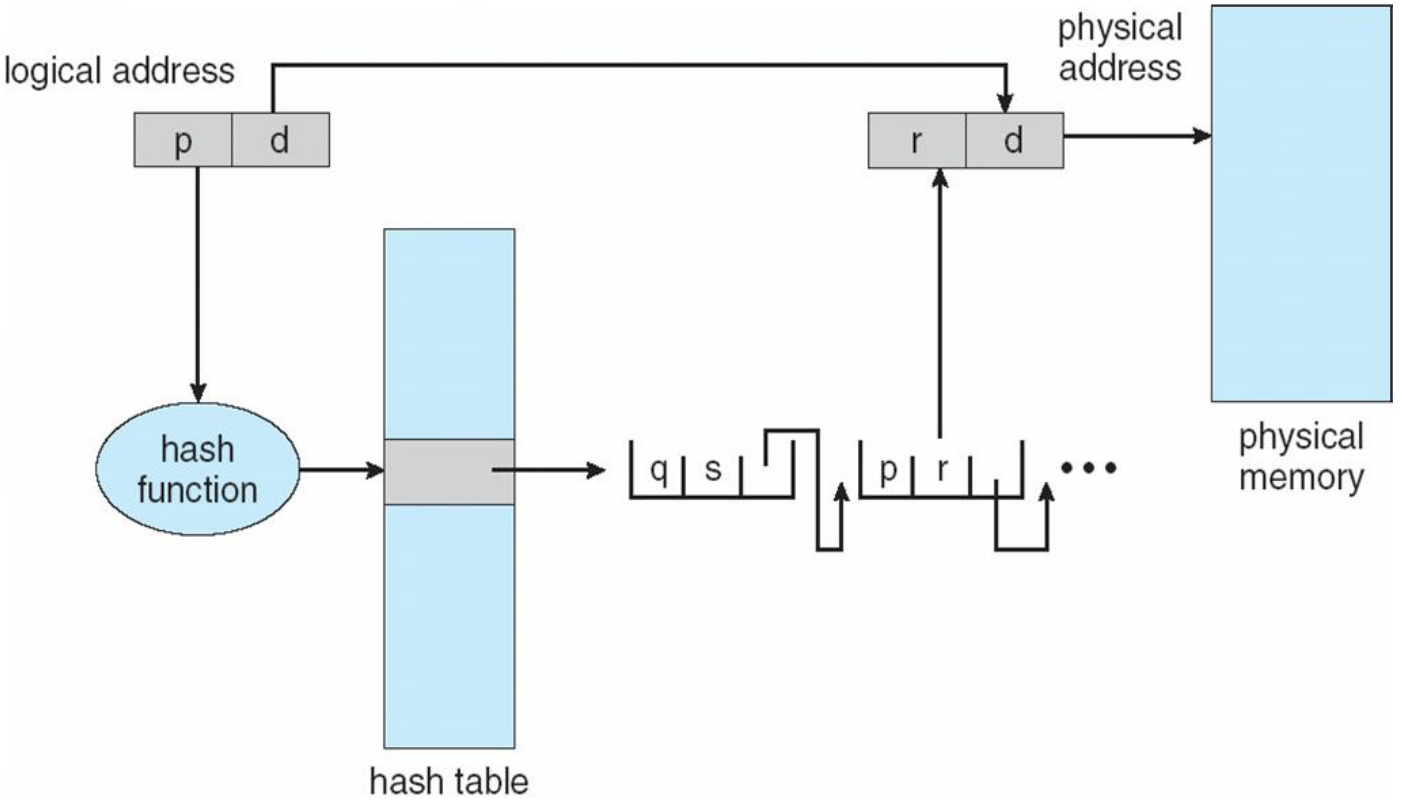
•Virtual page numbers are compared in this chain searching for a match

- •If a match is found, the corresponding physical frame is extracted

•Variation for 64-bit addresses is clustered page tables

- ➢Similar to hashed but each entry refers to several pages (such as 16) rather than 1
- ➢Especially useful for sparse address spaces (where memory references are non-contiguous and scattered)

Hashed Page Table



Inverted Page Table

•Rather than each process having a page table and keeping track of all possible logical pages, track all physical pages

•One entry for each real page of memory

•Entry consists of the virtual address of the page stored in that real memory location, with information about the process that owns that page

•Decreases memory needed to store each page table, but increases time needed to search the table when a page reference occurs

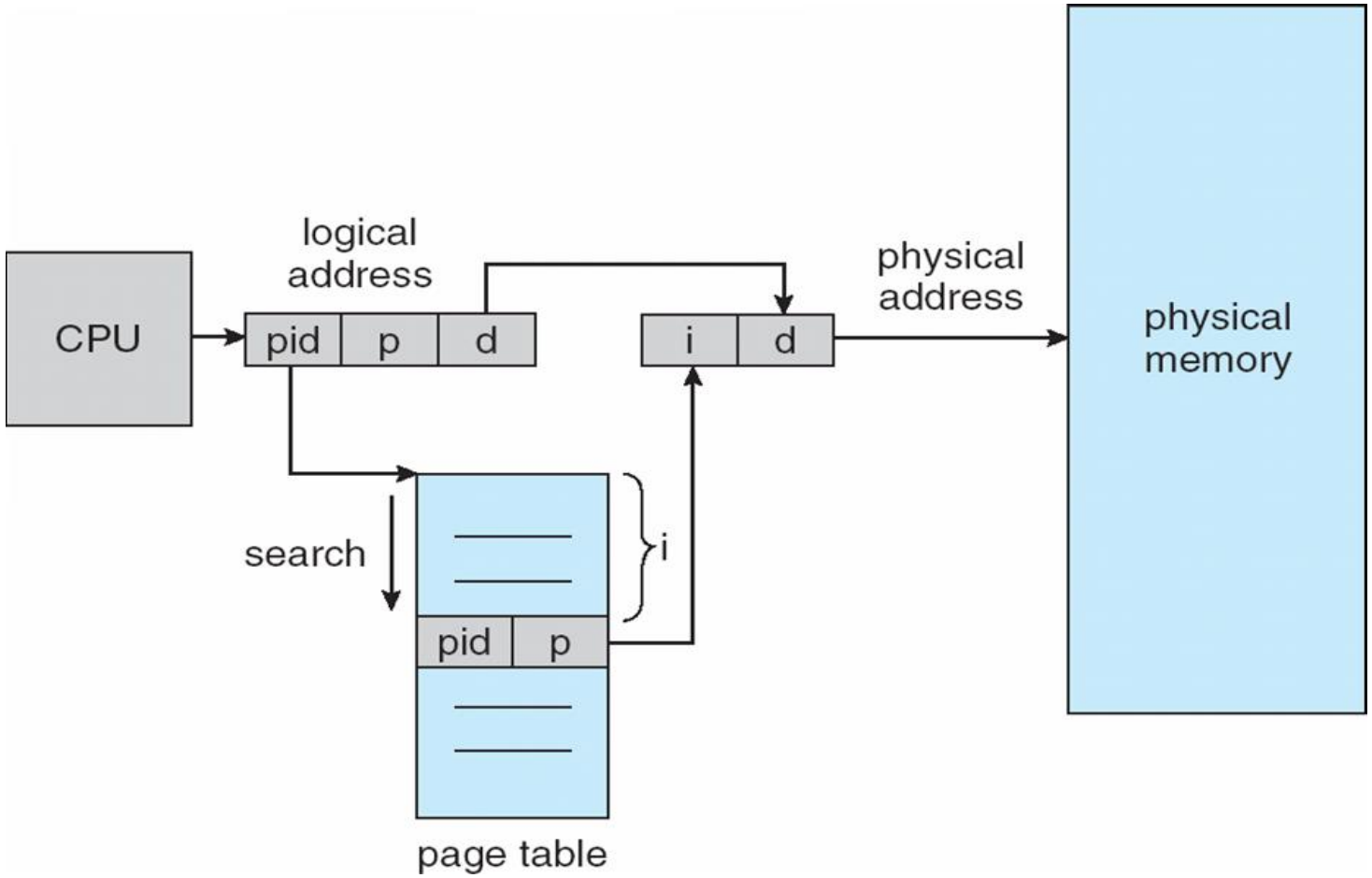
•Use hash table to limit the search to one — or at most a few — page-table entries

- ➢TLB can accelerate access

•But how to implement shared memory?

- ➢One mapping of a virtual address to the shared physical address

Inverted Page Table Architecture



MCQ

A memory buffer used to accommodate a speed differential is called…
A. stack pointer
B. cache
C. accumulator
D. disk buffer

The address of a page table in memory is pointed by…..
A. stack pointer
B. page table base register
C. page register
D. program counter

Program always deals with….
A. logical address
B. absolute address
C. physical address
D. relative address

page table contains…..
A. base address of each page in physical memory
B. page offset
C. page size
D. none of the mentioned

Operating System maintains the page table for:
A. each process
B. each thread
C. each instruction
D. each address